

FIG. 1

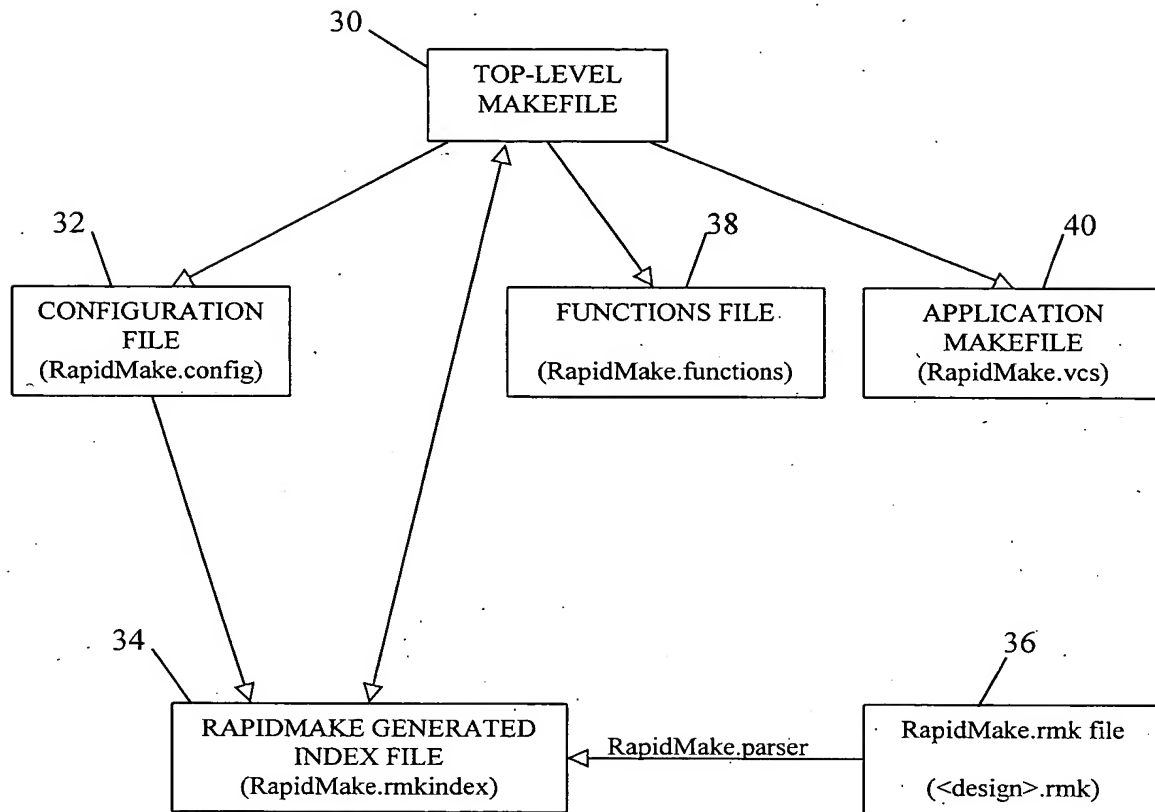


FIG. 2

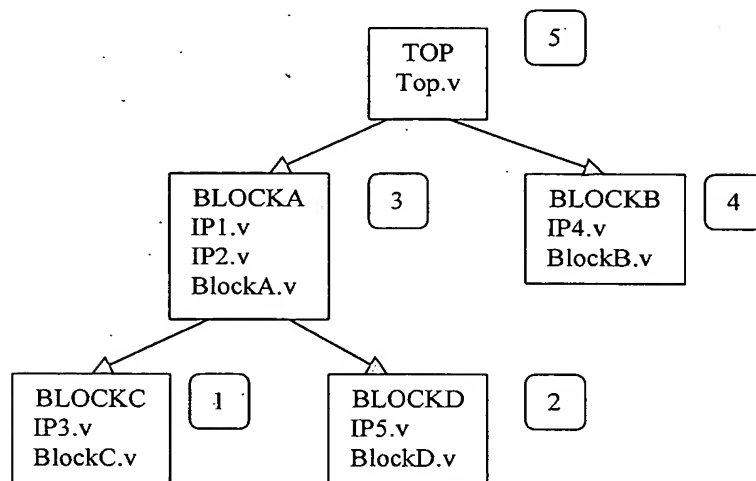


FIG. 3

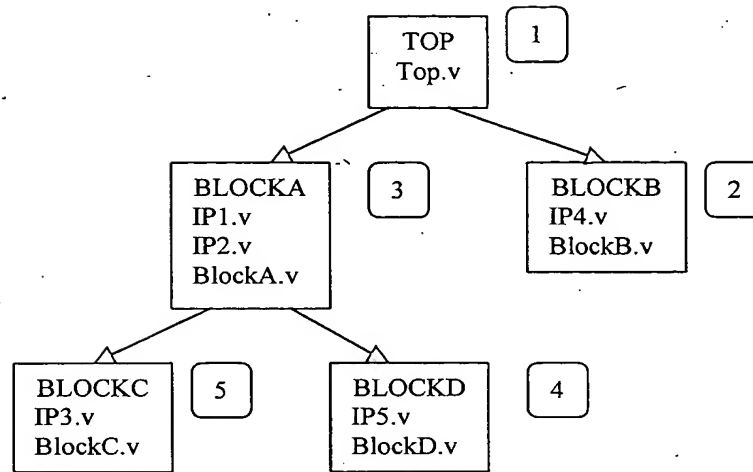


FIG. 4

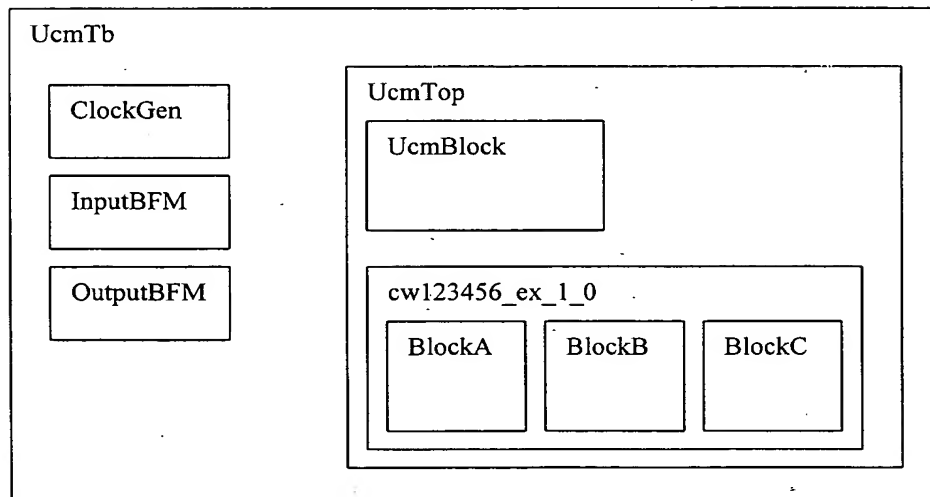
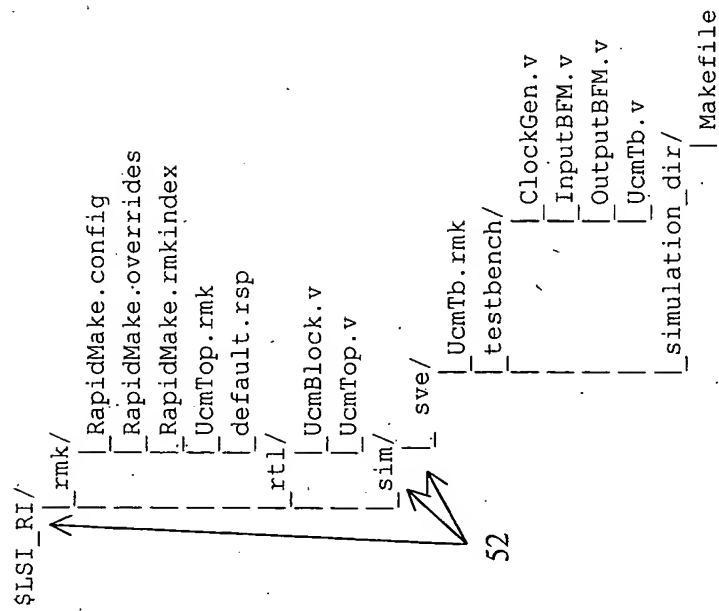


FIG. 5

```
$LSI_RW/tool/shared/lib/rmk/  
  | RapidMake.functions  
  | RapidMake.parser  
  | RapidMake.targets  
  | RapidMake.vcs  
  
$LSI_RS/RapidSlice_1810_1_0/  
  
$LSI_RRCW/cw123456_ex_1_0/  
  | prod/  
  |   | cw123456_ex_1_0.rmk  
  |   | rmk/  
  |   |   | default_rsp  
  |   |   | sim/  
  |   |   |   | rtlprot/  
  |   |   |   |   | verilog/  
  |   |   |   |   |   | modelsim/  
  |   |   |   |   |   |   | 5.7/  
  |   |   |   |   |   |   |   | cw123456_ex_1_0.vp  
  |   |   |   |   |   |   |   | vcs/  
  |   |   |   |   |   |   |   | 6.2/  
  |   |   |   |   |   |   |   |   | cw123456_ex_1_0.vp
```

FIG. 6



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FIG. 7

```
#Load Base RapidMake functions
#Location of the RapidMake library
RMK_HOME_DIR = ${LSI_RW}/tool/shared/lib/rmk

#Locate and include the makefile containing the base RapidMake
#functions
RMK_BASEFUNCTIONS_FILE = $(RMK_HOME_DIR)/RapidMake.functions
include $(RMK_BASEFUNCTIONS_FILE)

#RapidMake Configuration:
#Location of the RapidSlice
RMK_SLICE_DIR := ${LSI_RS}/RapidSlice_1810_1_0

#List of directories to search for other RapidMake files:
RMK_RAPIDMAKE_SEARCH_DIRS := ${LSI_RI}/rmk ${LSI_RI}/rwo/rmk \
    ${RMK_SLICE_DIR}/rmk ${RMK_HOME_DIR}

#Location of the makefile containing the base RapidMake targets
RMK_TARGETS_FILE := $(call find_file,RapidMake.targets, \
    ${RMK_RAPIDMAKE_SEARCH_DIRS})

#Location of the RapidMake.rmk parser makefile:
RMK_PARSER_FILE := $(call find_file,RapidMake.parser, \
    ${RMK_RAPIDMAKE_SEARCH_DIRS})

#Location to write autogenerated.rmk index:
RMK_INDEX_FILE := ${LSI_RI}/rmk/RapidMake.rmkindex

#Location of user overrides to autogenerated.rmk index:
RMK_INDEX_OVERRIDES_FILE := ${LSI_RI}/rmk/RapidMake.overrides

#List of directories to search recursively for .rmk files
RMK_INDEX_SEARCH_DIRS := ${LSI_RI} ${RMK_SLICE_DIR} ${LSI_RRCW}

#Tool Configuration
#Simulation
RMKSIM_LANGUAGE := verilog
RMK_SIM_TOOL := modelsim
RMK_SIM_TOOL_VERSION := 5.7
RMK_SIM_RAPIDMAKE_FILE = $(call find_file,RapidMake.${RMK_SIM_TOOL}, \
    ${RMK_RAPIDMAKE_SEARCH_DIRS})

#Define common shell utilities
RM = rm -f
CP = cp
#Defined so that the recursive make calls do not print directory info
MAKE = gmake --no-print-directory -r -R

#Boilerplate (user does not modify)
#Include autogenerated.rmk file index.
include $(RMK_INDEX_FILE)

#Include RapidMake base targets
include $(RMK_TARGETS_FILE)
```

FIG. 8

```
#Name of this module which will be used by other .rmk or routines in
#the RapidMake.functions to build the list of files.
RMK_MOD_NAME := CW123456_EX_1_0

#List of submodules used by this module by using the submodules module
#name. Do not include path names.
$(RMK_MOD_NAME)_SUB_MODS :=

#List of RTL files used in this module. The path from the .rmk file
location to the verilog file must be included.
$(RMK_MOD_NAME)_RTL_FILES := VLOG|sim|rtlprot/${RMK_SIM_LANGUAGE}/
    {RMK_SIM_TOOL}/${RMK_SIM_TOOL_VERSION}/cw123456_ex_1_0.vp

#Include the file to set up RapidMake Search Paths for this module.
include $(RMK_MOD_NAME)_RMK_DIR/rmk/default.rsp

###Boilerplate - DO NOT MODIFY
$(RMK_MOD_NAME)_RMK_VERSION := 1.00
include $(RMK_PARSER_FILE)
```

FIG. 9
cw123456_ex_1_0.rmk FILE

```
#Name of this module. This is used by other .rmk or routines in the
#RapidMake.functions to build the list of files.
RMK_MOD_NAME := UCMTOP

#List of submodules used by this module by using the submodules module
#name.
$(RMK_MOD_NAME)_SUB_MODS := CW123456_EX_1_0

#List of RTL files used in this module including the path from the .rmk
#file location to the verilog file.
$(RMK_MOD_NAME)_RTL_FILES := VLOG|UcmBlock.v\
    VLOG|UcmTop.v\
    MOD|CW123456_EX_1_0

#Include the file to set up RapidMake Search Paths for this module.
include $(RMK_MOD_NAME)_RMK_DIR/rmk/default.rsp

###Boilerplate - DO NOT MODIFY
$(RMK_MOD_NAME)_RMK_VERSION := 1.00
include $(RMK_PARSER_FILE)
```

FIG. 10
UcmTop.rmk FILE

```
#Name of this module.
RMK_MOD_NAME := UCMTB

#Do not include path information here. This should correspond to a
#RMK_MOD_NAME in another .rmk file.
$(RMK_MOD_NAME)_SUB_MODS := UCMTOP

#The path from the CustomerTb.rmk to the testbench files must be
#include.
$(RMK_MOD_NAME)_RTL_FILES := VLOG|testbench/ClockGen.v \
                             VLOG|testbench/InputBFM.v \
                             VLOG|testbench/OutputBFM.v \
                             VLOG|testbench/UcmTb.v \
                             YLIB|${LSI_RW}/lib3p/verilog/udps

##Boilerplate - DO NOT MODIFY.
$(RMK_MOD_NAME)_RMK_VERSION := 1.00
include $(RMK_PARSER_FILE)
```

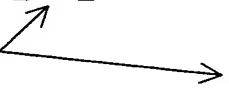
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FIG. 11
 TESTBENCH .rmk FILE
 (UcmTb.rmk)

```
#Common Configuration Options
#Define where to find the file containing common configuration options
#and functions.
RMK_CONFIG_FILE = $(LSI RI)/rmk/RapidMake.config

#Include common configuration options. This include causes the
#RapidMake.rmkindex file to be generated because the RapidMake.config
#file includes the RapidMake.functions file.
include $(RMK_CONFIG_FILE)

#Override RapidMake.config variables if the user wants to use a
#different revision of the encrypted RTL
RMK_SIM_TOOL      := vcs
RMK_SIM_TOOL_VERSION := 6.2

#Define and include top-level module.
RMK_TOP_MOD := UCMTB
ifdef RMKINDFX INCLUDED
  include $(call get_rmk_files, $(RMK_TOP_MOD))
endif

hdl_sim_compile:
    ${MAKE} -f $(RMK_SIM_RAPIDMAKE_FILE) compile \
    'FILES = $(call get_files_typed_recursive, \
    $(RMK_TOP_MOD), RTL,)'
```

FIG. 12
 TOP-LEVEL MAKEFILE


```
CW123456_EX_1_0_RMK_DIR := $(LSI_RRCW)/cw123456_ex_1_0/prod
CW123456_EX_1_0_RMK_FILE := $(CW123456_1_0_RMK_DIR)/cw123456_ex_1_0.rmk

UCMTOP_RMK_DIR := $(LSI_RI)/rmk
UCMTOP_RMK_FILE := $(UCMTOP_RMK_DIR)/UcmTop.rmk

UCMTB_RMK_DIR := $(LSI_RI)/sim/sve
UCMTB_RMK_FILE := $(UCMTB_RMK_DIR)/UcmTb.rmk
```

FIG. 13

RapidMake.rmkindex file

```
FILES = \
  VLOG|$(LSI_RI)/rtl/UcmBlock.v \
  VLOG|$(LSI_RI)/rtl/UcmTop.v \
  VLOG|$(LSI_RRCW)/cw123456_ex_1_0/prod/sim/rtlprot/vcs/6.2 \
    cw123456_ex_1_0.vp \
  VLOG|$(LSI_RI)/sim/sve/testbench/ClockGen.v \
  VLOG|$(LSI_RI)/sim/sve/testbench/InputBFM.v \
  VLOG|$(LSI_RI)/sim/sve/testbench/OutputBFM.v \
  VLOG|$(LSI_RI)/sim/sve/testbench/UcmTb.v \
  YLIB|$(LSI_RW)/lib3p/verilog/udps
```

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FIG. 14

OUTPUT LIST OF FILES